Claims

1. A MOS integrated one-way isolation coupler for use in a MOS integrated circuit on a semiconductor chip for providing an output signal in response to an input signal but electrically isolated therefrom, the isolation coupler comprising:

an inductor coil on the semiconductor chip for receiving the input signal and for generating a magnetic field in response to the input signal, the inductor coil having at least one turn and defining a central axis,

a MAGFET having a split drain defining a pair of drain portions wherein the current difference between the drain currents of the respective drain portions of the split drain is a function of the magnetic field to which the MAGFET is subjected, the MAGFET being located on the semiconductor chip relative to the inductor coil so that the current difference between the drain currents of the respective drain portions of the split drain is responsive to the magnetic field generated by the inductor coil in response to the input signal for providing the output signal, and the MAGFET is electrically isolated from the inductor coil so that the output signal is electrically isolated from the input signal.

2. An isolation coupler as claimed in Claim 1 in which the MAGFET is located relative to the inductor coil for providing the output signal to be proportional to the input signal.

3. An isolation coupler as claimed in Claim 1 in which the MAGFET defines a channel extending between the split drain and a source, the channel defining a channel plane, and the MAGFET is located relative to the inductor coil so that the magnetic field generated by the inductor coil in response to the input signal cuts the channel perpendicularly to the channel plane.

4. An isolation coupler as claimed in Claim 3 in which the MAGFET is located relative to the inductor coil with the central axis of the inductor coil extending substantially perpendicularly to the channel plane.

5. An isolation coupler as claimed in Claim 1 in which the central axis of the inductor coil extends substantially centrally through the channel of the MAGFET.

6. An isolation coupler as claimed in Claim 1 in which the MAGFET is located spaced apart from an axial end of the inductor coil.

7. An isolation coupler as claimed in Claim 1 in which the MAGFET is located close to an axial end of the inductor coil.

8. An isolation coupler as claimed in Claim 1 in which an electrical insulating layer is located between the MAGFET and the inductor coil for electrically isolating the MAGFET from the inductor coil.

9. An isolation coupler as claimed in Claim 8 in which the electrical insulating layer is a dielectric layer.

10. An isolation coupler as claimed in Claim 8 in which the electrical insulating layer is selected from any one or more of the following materials:

silicon dioxide,
silicon nitride, and
polyamide.

11. An isolation coupler as claimed in Claim 1 in which the MAGFET is located beneath the inductor coil.

12. An isolation coupler as claimed in Claim 1 in which the drain of the MAGFET is split so that the current difference between the drain currents of the respective drain portions is substantially zero when no current circulates in the inductor coil.

13. An isolation coupler as claimed in Claim 1 in which the inductor coil comprises a plurality of turns.

14. An isolation coupler as claimed in Claim 1 in which the turns of the inductor coil lie in a common plane.

15. An isolation coupler as claimed in Claim 1 in which the inductor coil is formed in at least two planes, each plane containing at least one turn of the inductor coil.

16. An isolation coupler as claimed in Claim 15 in which the planes containing the turns of the inductor coil are parallel to each other.

17. A semiconductor chip comprising:

an integrated circuit formed on the semiconductor chip,

a MOS integrated one-way isolation coupler on the semiconductor chip for providing an output signal to the integrated circuit in response to an input signal with the output signal electrically isolated from the input signal, the isolation coupler comprising:

an inductor coil on the semiconductor chip for receiving the input signal and for generating a magnetic field in response to the input signal, the inductor coil having at least one turn and defining a central axis,

a MAGFET having a split drain defining a pair of drain portions wherein the current difference between the drain currents of the respective drain portions of the split drain is a function of the magnetic field to which the MAGFET is subjected, the MAGFET being located on the semiconductor chip relative to the inductor coil so that the current difference between the drain currents of the respective drain portions of the split drain is responsive to the magnetic field generated by the inductor coil in response to the input signal for providing the output signal, and the MAGFET is electrically isolated from the inductor coil so that the output signal is electrically isolated from the input signal.

18. A semiconductor chip as claimed in Claim 17 in which the MAGFET is located relative to the inductor coil for providing the output signal to be proportional to the input signal.

19. A semiconductor chip as claimed in Claim 17 in which the MAGFET defines a channel extending between the split drain and a source, the channel defining a channel plane, and the MAGFET is located relative to the inductor coil so that the magnetic field generated by the inductor coil in response to the input signal cuts the channel perpendicularly to the channel plane.

20. A semiconductor chip as claimed in Claim 19 in which the MAGFET is located relative to the inductor coil with the central axis of the inductor coil extending substantially perpendicularly to the channel plane.

21. A semiconductor chip as claimed in Claim 17 in which the central axis of the inductor coil extends substantially centrally through the channel of the MAGFET.

22. A semiconductor chip as claimed in Claim 17 in which the MAGFET is located spaced apart from an axial end of the inductor coil.

23. A semiconductor chip as claimed in Claim 17 in which the MAGFET is located close to an axial end of the inductor coil.

24. A semiconductor chip as claimed in Claim 17 in which an electrical insulating layer is located between the MAGFET and the inductor coil for electrically isolating the MAGFET from the inductor coil.

25. A semiconductor chip as claimed in Claim 24 in which the electrical insulating layer is a dielectric layer.

26. A semiconductor chip as claimed in Claim 17 in which the MAGFET is located beneath the inductor coil.

27. A semiconductor chip as claimed in Claim 17 in which the drain of the MAGFET is split so that the current difference between the drain currents of the respective drain portions is substantially zero when no current circulates in the inductor coil.

28. A semiconductor chip as claimed in Claim 17 in which the inductor coil comprises a plurality of turns.

29. A semiconductor chip as claimed in Claim 17 in which the turns of the inductor coil lie in a common plane.

30. A semiconductor chip as claimed in Claim 17 in which the inductor coil is formed in at least two planes, each plane containing at least one turn of the inductor coil.

31. A semiconductor chip as claimed in Claim 30 in which the planes containing the turns of the inductor coil are parallel to each other.

32. A semiconductor chip as claimed in Claim 17 in which an amplifier is located on the chip for amplifying the current difference between the drain currents of the respective drain portions of the split drain for providing the output signal.

33. A method for one-way coupling an input signal to an integrated circuit on a semiconductor chip with the integrated circuit electrically isolated from the input signal, the method comprising the acts of:

fabricating an inductor coil on the semiconductor chip for receiving the input signal and for generating a magnetic field in response to the input signal, the inductor coil having at least one turn and defining a central axis,

fabricating a MAGFET on the semiconductor chip, the MAGFET having a split drain defining a pair of drain portions wherein the current difference between the drain currents of the respective drain portions of the split drain is a function of the magnetic field to which the MAGFET is subjected, the MAGFET being located on the

semiconductor chip relative to the inductor coil to form with the inductor coil a one-way isolation coupler, so that the current difference between the drain currents of the respective drain portions of the split drain is responsive to the magnetic field generated by the inductor coil in response to the input signal for providing an output signal to the integrated circuit in response to the input signal, and

electrically isolating the MAGFET from the inductor coil so that the output signal is electrically isolated from the input signal.

34. A method as claimed in Claim 33 in which the MAGFET is located relative to the inductor coil for providing the output signal to be proportional to the input signal.

35. A method as claimed in Claim 33 in which the MAGFET defines a channel extending between the split drain and a source, the channel defining a channel plane, and the MAGFET is located relative to the inductor coil so that the magnetic field generated by the inductor coil in response to the input signal cuts the channel perpendicularly to the channel plane.

36. A method as claimed in Claim 35 in which the MAGFET is located relative to the inductor coil with the central axis of the inductor coil extending substantially perpendicularly to the channel plane.

37. A method as claimed in Claim 33 in which the central axis of the inductor coil extends substantially centrally through the channel of the MAGFET.

38. A method as claimed in Claim 33 in which the MAGFET is located spaced apart from an axial end of the inductor coil.

39. A method as claimed in Claim 33 in which the MAGFET is located close to an axial end of the inductor coil.

40. A method as claimed in Claim 33 in which an electrical insulating layer is located between the MAGFET and the inductor coil for electrically isolating the MAGFET from the inductor coil.

41. A method as claimed in Claim 40 in which the electrical insulating layer is a dielectric layer.

42. A method as claimed in Claim 33 in which the MAGFET is located beneath the inductor coil.

43. A method as claimed in Claim 33 in which the drain of the MAGFET is split so that the current difference between the drain currents of the respective drain portions is substantially zero when no current circulates in the inductor coil.

44. A method as claimed in Claim 33 in which the inductor coil comprises a plurality of turns.

45. A method as claimed in Claim 33 in which the inductor coil is formed in a common plane, and the turns of the inductor coil lie in the common plane.